ECG-DEFF: ENHANCED CLOCK GATING BASED DOUBLE EDGE TRIGGERED FLIP-FLOP

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Abstract— ***In integrated circuit, total power consumption is due to the storage elements and clock distribution. Energy competence from the clock elements plays a biting role in low power circuit design. Double edge triggered flip-flop is one artistry for energy efficiency. It is keep the throughput as single edge triggered flip-flops. Because double edge triggered flip-flop using a semi of the clock frequency. Clock gating is another well accepted artistry to chop the dynamic power of otiose modules or cycles. However, combination of clock-gating with double edge triggered flip-flops to further reduce dynamic power consumption. But it is introduce an asynchronous data sampling error. Three special clock-gating techniques are evaluated to extenuate this issue. This technique has some limitation of reducing the error. In this paper by eliminating limitations and design the errors free circuits.***

Index Terms— Double edge trigger flip-flop, CLOCK-GATING, MosFET, FinFET, Asynchronous Data Sampling

1 INTRODUCTION

Developing the recital of mobile devices while keeping energy effectiveness is an important problem in present integrated circuits. The timing component is a major source of all the power consumption for a sequential system. In ICs a power efficient flip-flop is mostly designed for a basic element. Power-reducing techniques have been added to DETFFs in order to save the power dissipated on the clock tree. Clock-gating is one of the major techniques. For a huge digital system, clock-gating procedure is worn to reduce the power addicted on idle circuitry in the design. It can be technique for SETFFs or latches. To promote reduce the power utilization, Karimiyan et al., Tam et al., and Wang and Robinson unmitigated the clock-gating procedure for use with DETFFs.

The analysis of recent struggle to incorporate clock-gating technique with synchronous double edge-triggered system. For a clock-gated system, the internal clock manages the gated circuits. The internal clock is divided from the global clock, during the gated periods. If the internal clock is out of state with the global clock when the gating signal is conceal, then the internal clock signal switches directly to match the global clock. This interior clock switch is additional and asynchronized with the external clock, which generates an asynchronous data sampling, demonstrates by the output varying between clock edges. Since the problem is not constantly present, the analysis in this paper examines the specific conditions that generate the asynchronous data sampling.

Asynchronous sampling occurs when the grouping of clock-gating and double edge triggered techniques. In the previous analysis combine the clock gating with double edge trigger flip-flop. but not consider the power efficiently. In this paper reduce the power in the DETFF circuit with clock gating technique.

2 ASYNCHRONOUS MECHANISM WITH CLOCK GATING

In the discussion of the operational modes of the flip-flops, this paper promotes the following terms throughout the paper.

TERMS	SIGNALS
CLK	global clock signal
C	Gated clock signal
CG	clock
D	Input data signal
Q	output data signal

Table I

We think that all transitions on Q should be matched with an dynamic clock edge.

The asynchronous data sampling may basis data cover errors. Usually, clock gating is functional when D=Q, since it would be avoidable to sample the same signal value of stock into the flip-flop. Changeovers of D are used to uphold the CG signal. The C is the internal clock pulse that triggers the flip-flop. For the gating mode, the C keeps its value rather than provoking a dynamic edge. For the non-gating mode, C shift after the changeover on CLK. However, if D varies while C is not equivalent to CLK , then an asynchronous data changeover may happen that is observed on the output.

Fig 1 illustrates an example of a data error convinced by the non synchronous data sampling. When D changes from 0 to 1, CG is hide to allow the flip-flop to run usually. The input had a pulse between two clock limits that does not overlie with the setup and hold time.

According to the meaning of flip-flops, the input switch that happens in Fig. 1 should not be experimental at the output. However, due to the asynchronous data sampling related

with clock-gated DETFFs, this input pulse will be moved to the output as if the flip-flop was a sheer latch.

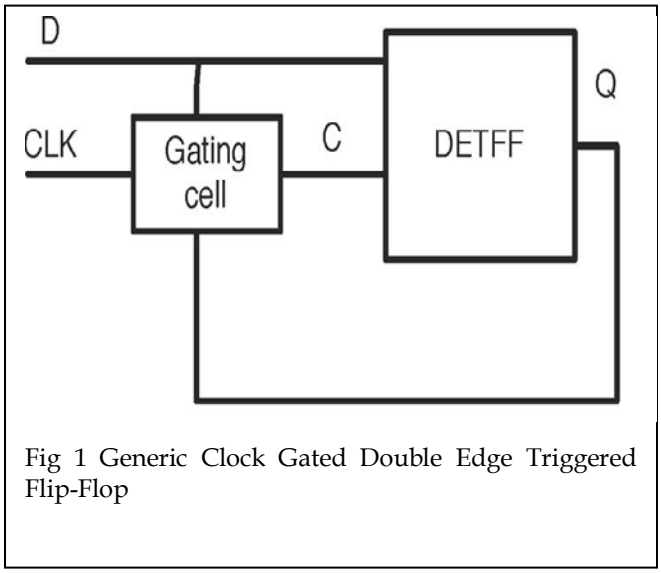

Fig 1 Generic Clock Gated Double Edge Triggered Flip-Flop

For double edge-triggered D-type flip-flops, there are eight potential when allowing for factors of: (1) the next input D, (2) the present output Q, and (3) the active clock edge. Four scenarios hold the prior value, and the other four enable a data transition. In this paper, we focus on the four grips that permit a data changeover. When clock gating is swinging off, there will be a half percentage possibility to have an asynchronous data transition.

Different applications of a DETFF with clock gating explain the principle of how the asynchronous data sampling produce. However, the asynchronous data sampling proportion the same root cause, namely the break between the global and internal clock.

If the internal clock alters from the global clock when clock gating is canceled, then the internal clock episode is broadcast directly.

3 ASYNCHRONOUS DATA SAMPLING OCCURS IN DOUBLE EDGE TRIGGERED FLIP-FLOP

3.1 Asynchronous Sampling in the Gated Double Edge-Triggered Flip-Flop with Transmission Gate (G_DETFF)

The Latch-MUX structure using transmission gate is the building blocks of this flip-flop. It's having two data paths with coordinating connected. In the rising edge upper path is triggered and vice versa. The input and output of the two paths preferably monitor, which means that the input is consistently preloaded into the flip-flop. Instead of generating a pulse for every changeover, the clock gating part in A low-power double edge-triggered flip-flop with transmission gates and clock gating was designed to toggle C whenever the data input changed in order to eradicate power consumption for unneeded transitions.

During the gating periods, the internal C conserves the last used value before being gated. It inhibits the clock signal in an energetic way. So it's improved clock gating techniques for DETFF.

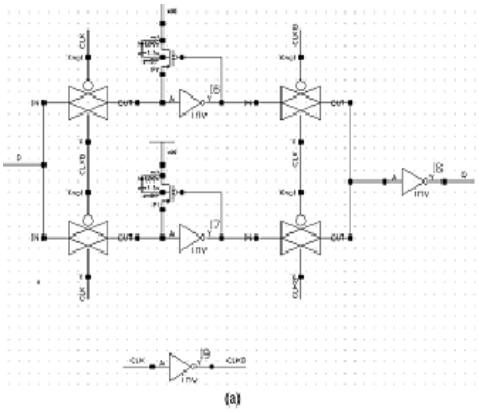

Fig 2 a) Gated double edge trigger flip-flop

If C ≠ CLK, when the circuit deactivates the clock-gating function, then the error signal appears for the Gated-DETFF. In the output of Gated-DETFF that shows the existence of the asynchronous sampling issue within the design. Two error signals occurred, where D changes when CLK ≠ C.

3.2 Asynchronous Sampling in Low-Power Dual-Edge Triggered State Retention Scan Flip-Flop (DET SRSFF)

Pulse generator and scanable static latch are the building blocks of Dual edge triggered state retention scan flip-flop (DET SRSFF). Scanable static latch gives an absence of leakage current. DETSRSFF has many asset, but here our inquiry only targets on the flip-flop function.

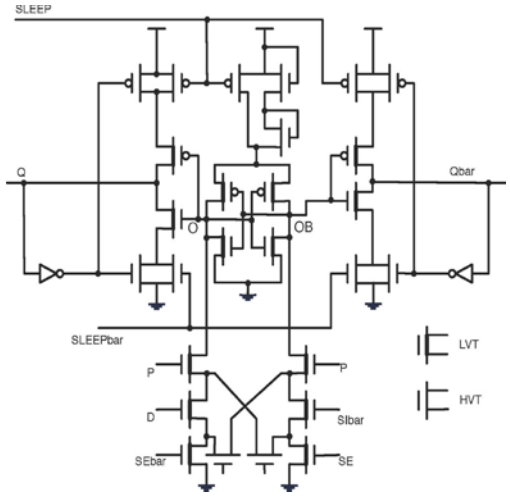

Fig 3 Double Edge Triggered State Retention Scan Flip-Flop(DETSRSFF)

When the logic level is high, the latch part has enabling. Floating output is avoided by the leakage feedback buffer (LFB). It's operates two modes which is normal when SE = 0 and test mode when SE = 1. The pulse generator act as the clock gating part.

3.3 Asynchronous Sampling in the Double Edge-Triggered Half-Static Clock-Gated D-Type Flip-Flop (DHSCGFF)

Two flip-flops and MUX is the building blocks of a DHSCGFF. The clock-gating signal is nothing but matching the value of input D and output, and is hooked up to a switch M2 that curbs the signal path of the global **CLK** to the internal clock. C and Cbar are an equivalent signal, these signals are the internal clock signals generated from the inverter chain. Master Latch 1 and Master Latch 2 are the data paths that are shown in the figure. The sliding edge of C , the upper part is selected. The elevating edge of C, lower part is selected. The gate is dormant, the gated signal R = 0. When CLK = 0, the input data transposed.

In that condition C = 1 and Cbar = 0. Nonsynchronous clock edge of generating flip-flop, provoking the asynchronous data sampling. The gated signal C return to 0, after specific data changeover and halts low until the next changeover. In the standby mode, master Latch 1 is ever ON. When the data signal is altered, master Latch 2 is ever be started first.

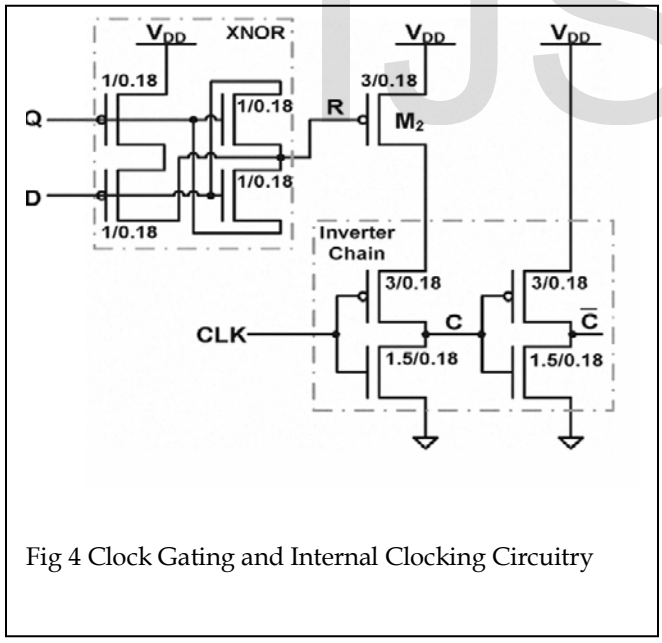

Fig 4 Clock Gating and Internal Clocking Circuitry

In variation to other Latch-MUX double edge-triggered flip-flops that position a logic keeper at Node X2 to avoid soaring nodes, Tam's design added switches MB1 and MB2 into the latch that deliberately isolate Nodes X1 and X2. According to the figure, after the input switches and before switch MA2 turns OFF, the value of Node X0 starts to adjust. When the lower path is triggered, the switch MC2 turns ON,MB2 and MA2 turn OFF, and soaring Node X2 trips the output.

For those input appearances that occur during CLK =1, the lower path would not be triggered until CLK=0. When it is triggered, X0 has quiet enough charge and is strong enough to drive X2 and allow the X2 signal to pass to X3. For transitions on input D that occur during CLK =0, a non synchronous pulse is provoked on internal clock. Then before switch MA2 turns OFF, there is only a very precise amount of time for Node X0 to charge or discharge.

If the value of X0 is active enough to flip the nodes to the output, then a nonsynchronous transition will appear at the output. Otherwise, if the first provoke of the lower path has not strongly passed the input D to the output, then the upper path deliver as a substitute that will be triggered at the next falling edge of C bar.

4 METHODS TO AVOID ASYNCHRONOUS SAMPLING

Method A: When the gating signal is de-asserted, only resume the connection of **CLK** to C during CLK=C, which avoids the asynchronous transition in .

Method B:Always force the clock-gating signal to synchronize with the **CLK**.

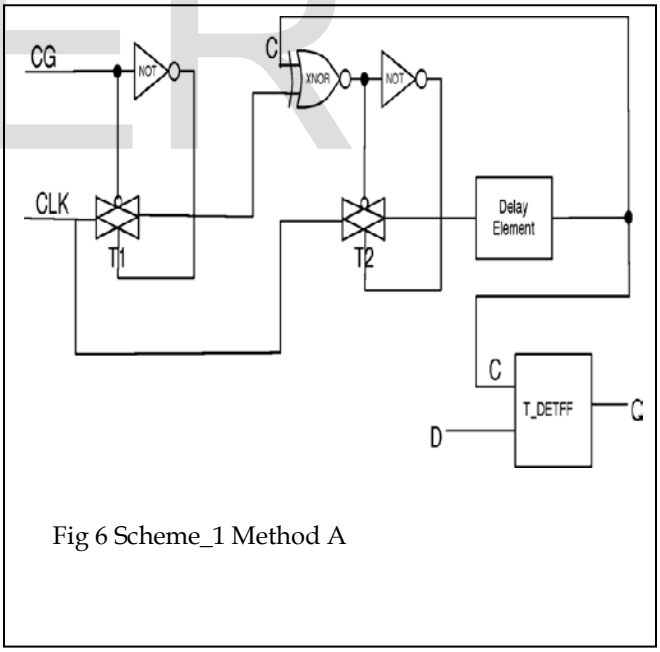

Fig 6 Scheme_1 Method A

From the Fig. 10, the **CLK** is controlled by the comparison of D and Q . If D has returned for the last cloc k change over and is various from Q , then **CLK** will pass to the second comparator to match with the C . This CLK & C comparator force the switch T2 between the C and **CLK**.

This second comparator blocks the asynchronous sampling appears in this application. Asynchronous sampling arise when D differs at the stage that CLK differs from. However, with the second CLK&C comparator in Fig. 10, the switch T2

will halt OFF when CLK not equal to C , and C will concur with CLK. In the next half cycle where CLK = C, the switch T2 turns ON, but considering they are identical, the flip-flop will not be caused before C changes, which pursue CLK when T2 is ON.

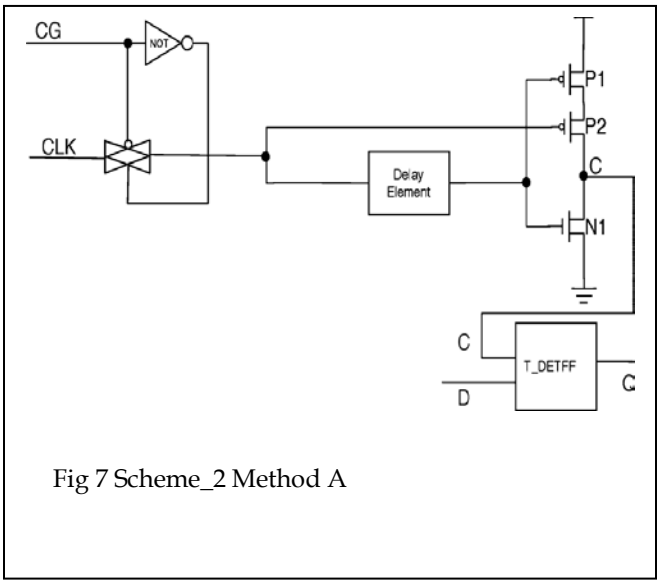

Fig 7 Scheme_2 Method A

From the Fig. 11, the nonsynchronous sampling is bypassed by the following mechanism. The C regularly halts at 0. When D changes while the CLK is 1, transistor P2, the one adjacent to CLK, will be turned OFF shortly, and C will stand the same. When CLK return to 0 , P2 is ON, and because of the delay element, P1 will halt ON for the time desired to provoke the flip-flop.

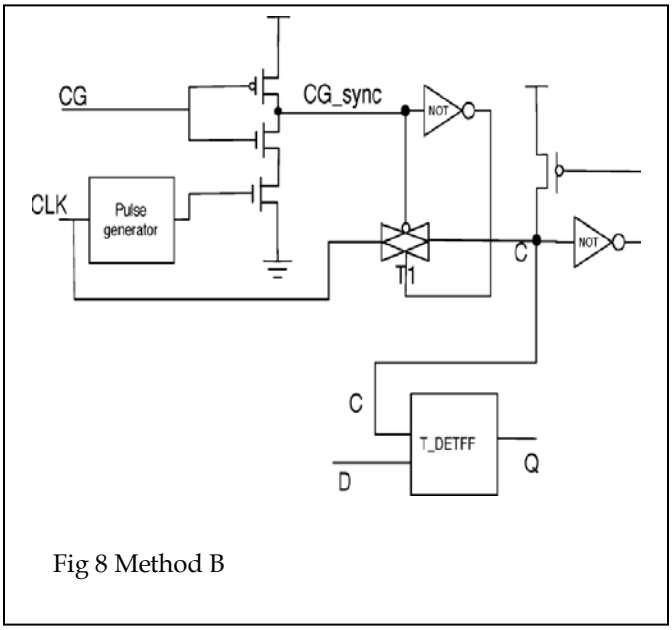

Fig 8 Method B

From the Fig. 12 is the employment of Method B. The pulse generator encounter and produce a positive pulse for whole edge of the **CLK**. No matter when D shifts, against the comparator's result are ready directly, the ON signal of the transmission gate T1 only produces at clock edges. So C and **CLK** are meshed, and the non synchronous sampling is bypassed in this design. The generated pulse width has to be deep full to grand the flip-flop with taking data successfully.

From the earlier analysis, Scheme_2 has improved act on power consumption. However, a watchful analysis of the three solutions shows that Method B is fit for real executions. Because Method A has a pulse of the internal C for each data switching, the DETFF will be provoked twice. Based upon the global **CLK**, the DETFF only provokes at one type of clock edge, which cause it a DETFF that act like a single-edge-triggered flip-flop (SETFF). The profit of Method B is that the internal C only dial once for every changeover. But Method B has a un-gated pulse generator. One way to amortize the power addicted / not consider the power efficiently. In this paper reduce the power in the DETFF circuit with clock gating technique.

CONCLUSION

As the basic aspects of a computing system, the flip-flops are typically the destination for development and enhancement. Because of the high need of mobile devices on power efficiency, a variety of power reduction techniques showed. DETFF and clock gating are two techniques to lower the dynamic power consumption, and both of them are successfulwhen used separately. However, when applying clock gating into aDETFF, error may occured at the output between clock edges due to asynchronous data sampling.

The previous analysis of double edge triggered with clock gating is given the solution for asynchronous data sampling.But the problem was not fully omitted inprevious paper here the power consumption of double edge triggered flip-flop is very high.Using FinFET over the mosFET the power and area are reduced. So focus on the FinFET technology is more advantageous than previous one. The methods of avoiding error signal which is designed with FinFET and analysis the power and area.

The future work is going to combine all the error omitting circuits for our convenience. The main object is that all the three circuit having capabilities of working in power,area and delay. So we have to form a circuit for whole three.

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